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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,426	01/29/2004	Koji Uchida	3408.69382	4566

7590 03/15/2006

Patrick G. Burns, Esq.  
GREER, BURNS & CRAIN, LTD.  
Suite 2500  
300 South Wacker Dr.  
Chicago, IL 60606

EXAMINER

MARTINEZ, DAVID E

ART UNIT PAPER NUMBER

2181

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/767,426	<b>Applicant(s)</b> UCHIDA ET AL.	
	<b>Examiner</b> David E. Martinez	<b>Art Unit</b> 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 29 January 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☒ Claim(s) 2-6 and 10-14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

*St. J. M. Fleming*  
FRITZ FLEMING  
Supervisory PRIMARY EXAMINER  
GROUP 2100  
AU 2181  
3/13/2006

#### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 1/29/04.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Objections*

Claims 3,5,6,11,13 and 14 are objected to because of the following informalities: The acronym "LBA" in the claims should be spelled out at least during its first use, in order to show its appropriate meaning. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said plurality of logical units" in lines 11-12. There is insufficient antecedent basis for this limitation in the claim. In addition, lines 10-12, the term "wherein when said host sends an I/O request to concatenation logical unit concatenating said plurality of logical units" also renders the claim indefinite. Is there lack of antecedent basis for the "concatenation logical unit"? or is there a missing "a" at the end of line 10 and thus introducing a first instance of a concatenation logical unit? Furthermore in line 16, the term "then sends the I/O request to another controller..." is also indefinite. Who is sending the I/O request to another controller? Is it the first controller what received the first request from the channel adapter? Or is it the channel adapter who sends another I/O request to a second controller? Also in line 16, the term "another controller" makes the term unclear. It is not understood if the "another controller" is a recitation of a new controller which was not previously claimed, or if it is referring to one of the controllers that are included in the "plurality of controllers" in line 6. Lastly, in line 17, is the term "another logical unit" referring to one of the

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“plurality of physical units” in line 5, or is it a new instance of a new logical unit? The preamble makes it understood that there is only one logical unit in line 4.

With regards to claim 9, it suffers from the similar deficiencies as claim 1 and thus is rejected under the same rationale.

Due to Claims 2-8 and 10-16 being dependent from independent claims 1 and 9 respectively, they suffer from the same deficiencies as their parent claims and thus are rejected under the same rationale.

Due to the vagueness and a lack of clear definiteness in the claims, the claims have been treated on their merits as best understood by the examiner.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 7-9, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of US Patent No. 5,423,046 to Nunnelley et al. (hereinafter Nunnelley).

1. With regards to claims 1 and 9, AAPA teaches a storage control apparatus [figs 12, 13] for accessing data of a logical unit [fig 12 elements 140, 150, fig 13, elements LU0 containing elements 140, 150], which is comprised of a single or a plurality of physical units [page 2 lines 17-19], by a request from a host [data in a logical volume comprised of disk devices is always accessed by requests to write or read, page 3 lines 4-11], comprising:

a channel adapter [figs 12 and 13, elements 120,122,124,126] for interfacing with said host [figs 12 and 13, element 100]; and

a plurality of controllers [figs 12 and 13, elements 128, 130] which charge each one of the plurality of logical units [page 2 line 27 to page 3 line 3],

wherein when said host [figs 12 and 13, element 100] sends an I/O request [data in a logical volume comprised of disk devices is always accessed by requests to write or read, page 3 lines 4-11] to concatenation logical unit [fig 13 element 'Concatenation LU0'] concatenating said plurality of logical units [fig 13 elements 140 and 142], said channel adapter [figs 12 and 13, elements 120,122,124,126] sends an I/O request to one controller [host requests data in concatenation LU0, page 3 lines 4-11] which charges one logical unit constituting said concatenation logical unit [page 2 line 27 to page 3 line 3], out of said plurality of controllers [fig 13 elements 128 and 130] to execute the I/O processing in said one controller [page 3 lines 1-11].

AAPA teaches all of the above limitations except for then sending the I/O request to another controller which charges another logical unit constituting said concatenation logical unit to execute the I/O processing in said other controller. However, Nunnelley teaches sending I/O requests to a plurality of controllers [column 2 lines 19-54, column 9 lines 39-43] to access data from a concatenation logical unit [column 4 lines 4-16, column 4 line 48 to column 5 line 4, column 8 line 43 to column 9 line 43, accessing a dataset from a cluster, a cluster being a concatenation logical unit comprised of a plurality of physical disks] for the benefit of using a plurality of controllers to increase throughput while accessing a concatenation logical unit, increasing overall system reliability by providing redundancy and sharply decreasing data access times [column 1 lines 40-46].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine AAPA and Nunnelley to then send the I/O request to another controller which charges another logical unit constituting said concatenation logical unit to execute the I/O

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processing in said other controller for the benefit of using a plurality of controllers to increase throughput while accessing a concatenation logical unit, increasing overall system reliability by providing redundancy and sharply decreasing data access times.

2. With regards to claims 7 and 15, AAPA teaches the storage control apparatus according to claim 1, wherein said each controller comprises:

a cache memory for storing a part of the data of said logical unit which the controller charges [page 3 lines 1-11]; and

a processing unit for executing I/O processing using said cache memory according to said I/O request [page 3 lines 1-11].

3. With regards to claims 8 and 16, AAPA teaches the storage control apparatus according to claim 1, wherein said channel adapter is constituted by a plurality of channel adapters [Figs 12 and 13 elements 120,122,124,126] for connecting said plurality of controllers [figs 12,13 elements 128, 130, page 2 lines 9-15].

***Allowable Subject Matter***

Claims 2-4, 5-6, 10-12, and 13-14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As per claims 2-4 and 10-12, the prior art of record fails to disclose of fairly suggest: a controller judging whether an I/O request is an I/O request extending over to another controller which charges another logical unit constituting a concatenation logical unit, and the controller responding to a channel adapter with the results of the judging.

As per claims 5-6 and 13-14, the prior art of record fails to disclose of fairly suggest: a table, for storing controllers corresponding to each logical unit, the LBA range of each logical

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unit, the logical units constituting a concatenation logical unit, and selecting a controller of the corresponding logical unit when an I/O request is received from a host.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 6,948,010 to Somers et al. teaches two controllers (a master controller and a slave controller) that transfer different portions of a memory block from one source location to a target location. One master controller configures the slave controller with the information about the portion of data to fetch and then concatenating the data at the target location.

US Patent No. 6,009,481 to Mayer teaches channel adapters connected to a host, the channel adapters also connected to controllers that access data from drives.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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DEM

Supervisory

*Fritz Fleming*  
FRITZ FLEMING  
PRIMARY EXAMINER  
GROUP 2100

42281

3/13/2006